

Atty. Docket No. OPP031058US
Serial No: 10/736,063

Amendments to the Claims

Please amend Claims 1, 3-7, and 9-12, cancel Claim 13, and add new Claims 14-21 as shown below. This listing of Claims replaces all prior versions and listings of the Claims in this application.

Listing of Claims

1. (Currently Amended) A method of forming a gate in a semiconductor device, the method comprising:

forming a trench in a semiconductor substrate;

forming on a semiconductor substrate a gate oxide layer and then on the semiconductor substrate;

forming on the semiconductor substrate a sacrificial layer;

selectively etching the sacrificial layer to form a sidewall opening over an area of the semiconductor substrate including the trench;

forming a polycrystalline silicon layer on an area of the gate oxide layer exposed through the sidewall opening and on the sacrificial layer;

performing anisotropically etching of the polycrystalline silicon layer such that sidewall gates are formed by remaining portions of the polycrystalline silicon layer on sidewalls of the sidewall opening, a width of the sidewall gates corresponding to a desired width of a gate; and

removing the sacrificial layer.

2. (Original) A method as defined by claim 1, wherein the sacrificial layer comprises a nitride layer.

3. (Currently Amended) A method as defined by of claim 2, wherein removing the nitride layer is removed using comprises a wet etching process.

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4. (Currently Amended) A method as defined by claim 1, wherein removing the sacrificial layer is removed using comprises a wet etching process.

5. (Currently Amended) A method as defined by claim 1, wherein anisotropically etching of the polycrystalline layer comprises an etch-back process.

6. (Currently Amended) A method as defined by claim 1, wherein the width of the sidewall gates is determined by a thickness of the sacrificial layer determines widths of the sidewall gates.

7. (Currently Amended) A method as defined by claim 1, wherein the width of the sidewall opening formed by selectively etching the sacrificial layer corresponds to a width from one gate to an adjacent gate.

8. (Original) A method as defined by claim 7, wherein the sacrificial layer comprises a nitride layer.

9. (Currently Amended) A method as defined by claim 8, wherein removing the nitride layer is removed using comprises a wet etching process.

10. (Currently Amended) A method as defined by claim 7, wherein removing the sacrificial layer is removed using comprises a wet etching process.

11. (Currently Amended) A method as defined by claim 7, wherein anisotropically etching of the polycrystalline layer is comprises an etch-back process.

12. (Currently Amended) A method as defined by claim 7, wherein the width of the sidewall gates is determined by a thickness of the sacrificial layer determines a width of the sidewall gates.

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13. (Cancelled)

14. (New) The method of claim 12, wherein widths of the sidewall gates correspond to a desired width of a gate.

15. (New) The method of claim 1, wherein anisotropically etching the polysilicon layer comprises over etching the sidewall gates to a minimum width.

16. (New) The method of claim 5, wherein the etch-back process comprises over etching the sidewall gates to a minimum width.

17. (New) The method of claim 11, wherein the etch-back process comprises over etching the sidewall gates to a minimum width.

18. (New) The method of claim 1, further comprising depositing a photoresist layer on the sacrificial layer.

19. (New) The method of claim 18, further comprising patterning the photoresist layer to form an opening exposing a predetermined area of the sacrificial layer.

20. (New) The method of claim 19, wherein the opening comprises an area on the substrate from where one sidewall gate will be formed to where an adjacent gate will be formed.

21. (New) The method of claim 19, wherein the opening encompasses an area on the substrate from where one sidewall gate will be formed to where an adjacent gate will be formed.